REMARKS

Claims 1-15 are presently pending and stand rejected. Claims 16-18 are cancelled without prejudice. Claim 19 is added.

Claims 1-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Malladi in view of Sugiyama.

Claims 14 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Malladi in view of Sugiyama and Son.

Claims 1 and 7 were rejected under 35 U.S.C. § 103(a) as being obvious from Malladi in view of Sugiyama, Hrusecky, and AAPA. Examiner has indicated that "Malladi is silent in regards to writing a start code starting at a byte in a middle portion of a data word in a memory. However, Sugiyama teaches writing a start code starting at a byte in a middle portion of a data word in a memory. However, Sugiyama teaches writing a start code starting at a byte in a middle portion of a data word in a memory ([0123] and fig. 13A and 14).".

Assignee respectfully traverse the rejection. Although in Figure 13A, "each code boundary is byte assigned", Paragraph 0119, there is no teaching that the byte is "in a middle portion of a data word". Moreover, 0123 teaches that "Fig 14 shows a real example of a header of an MPEG stream". Note that since Figure 14 merely describes the stream, without any reference to how the stream is stored in memory, the foregoing does not teach "a start code starting at a byte in a middle portion of a data word in a memory".

Examiner has responded that:

> As shown in Figure 13A, in each of the higher layers from the sequence layer to the picture

layer, each boundary is byte assigned [0119] and fig. 13A.
Sugiyama teaches fig. 14 is a schematic diagram showing a real example of a header of an MPEG stream according to a first embodiment [0052]. Further disclosed is that a stream that is output from the selector 306 is temporarily written to a memory 307 and a memory 313. The variable length code encoder (VLC) 308 controls the addresses of the stream written in the memory 307 so as to convert the stream into an MPEG stream 0277. Since Sugiyama discloses the stream can be written in the memory and the VLC controls the address of the stream, it is clear to the examiner that Sugiyama discloses the stream is written to an address in memory. Therefore, since Sugiyama discloses the start codes are byte assigned and the streams can be written in the memory and VLC controls the address of the stream, it is clear to the examiner Sugiyama disclose the writing a start code in the middle portion of a data word.

Assignee respectfully maintains traverse. Although Examiner characterizes Figures 13A and 14 are shown as a stream and not stored in a memory in Figures 13A and 14. Although the Office Action characterizes it as "byte-assigned", Figures 13A and 14 are not mapped to memory. It appears to be an implicit assumption that Sugiyama teaches storing what is depicted in Figure 14 consecutively. This is not the case. For example, "The memory 313 is a memory that delays a slice header and macroblock header." 0277. Sugiyama also notes that "The data that has been rearranged and read from the memory 307 is supplied to the VLC 308." 0280. Thus, even if what is depicted in Fig. 14 is stored in memory, Sugiyama does not store it consecutively. Thus even if the byte assignment taught a start code in the middle of a word, it does not follow that Sugiyama teaches storing the same in the middle of a memory word.

Accordingly, Assignee respectfully submits that neither of Sugiyama or Malladi teach the foregoing elements. Accordingly, Assignee respectfully requests withdrawal of the rejections to claims 1 and 7 as well as the dependent claims.

Additionally, claim 14 was rejected over the combination Malladi, Sugiyama, and Son. Examiner has indicated that Son discloses a first masking register for discarding a portion of a first data structure that precedes the starting address (Son, Column 8, lines 53-56)".

Assignee respectfully traverses the rejection. Son, Column 8, lines 53-56 merely states that "Upon beginning a next start code 405 detection operation to detect next start code 405, multi-standard start code detector system 300 rapidly discards entire bit groups until detection of at least a portion of next start code 405." Assignee traverses because the foregoing does not teach the claimed "masking register".

Examiner has responded that "an ALU has been able to perform both the logical operation of AND/OR on the chip level." Assignee maintains traverse because there is no teaching in Malladi that the ALU actually is used to perform the masking operation. Accordingly, Assignee respectfully traverses the rejection to claim 14 and requests allowance for claim 19.

CONCLUSION

For at least the foregoing reasons, Assignee submits that each of the pending claims are now in a condition for allowance. Accordingly, Examiner is requested to pass this case to issuance.

It is believed that all monies for the actions described herein are provided with this correspondence. To the extent that additional monies are required for any of the actions requested in the correspondence, Commissioner is authorized to charge such fees and credit any overpayments to deposit account 13-0017.

Respectfully Submitted

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